IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE UNITED STATES PATENT	I AND	TRADEMAK	KOFFICE Surley	
OIPE Inre Application of:	§ §	Group Art Uni	/ 11-101/	
DEC 0 8 1998 F Ravi Iyer	§ §	Examiner:	Nguyen, T.	
Filed: April 14, 1998  For: PLANARIZATION USING PLASMA OXIDIZED AMORPHOUS SILICON	8 8 8	Atty Docket:	MICS:00152/FLE 93-118.02	

CERTIFICATE OF TRANSMISSION AND MAILING 37 C.F.R. 1.8

GAV

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December 3, 1998

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

## **AMENDMENT**

In response to the Official Action mailed on August 3, 1998, please amend the abovereferenced application as follows:

IN THE CLAIMS  Please cancel claim 1 without prejudice.  Please amend claims 18, 22, and 23 as set forth below:	RECEIVED 98 DECITAR 8: 55
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18 (once amended). A method of manufacturing an integrated circuit, the method

comprising the steps of: